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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,375	07/25/2001	Hideyuki Furukawa	100353-00069	3493

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,375	FURUKAWA, HIDEYUKI	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **1 to 9** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No: 2001-017603 filed on 01/25/2001.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included and excluded by the claim language with the use of the phrase: "information about whether ECC correction is possible". This claim is an omnibus type claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim **1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (U.S. PN: 6,058,047) in view of Ma et al. (U.S. PN: 5,956,473).

As per claim **1**, Kikuchi discloses/teaches a semiconductor memory device including a semiconductor memory having a memory region divided into a plurality of blocks including a backup blocks, the number of writes to each block being limited, and a memory controller for reading data from the semiconductor memory so as to check an error in the data read from each block, and correcting the error if it is correctable. Further, the memory controller includes a counter for counting the number of correctable errors detected for each block, transferring the data of the corresponding block to the backup block when the number of errors detected reaches a preset value, and inhibiting re-use of the block (see abstract and col. 1, lines 6-14). Kikuchi teach that each block includes a data region in which data is written and a redundant region in which information indicating the quality of the block, and administrative information such as ECC (error correcting code), used for detecting and correcting an error occurred in data written and further the ECC used for a purpose that a 1-bit error detected and corrected, and 2-bit error only detected in which designated as a defective block and the re-use thereof is inhibited (see col. 1, lines 45-54 and claim 1). Further, Kikuchi discloses or teaches an inhibiting unit which

monitors whether or not the count reached a preset value, and if so, transfers the data to the backup block and inhibits the re-use of the block as a defective block (see col. 2, lines 45-52). Kikuchi **do not explicitly** teach marking a defective block. **However,** Ma et al. in an analogous art teach a method for providing defect management, wear leveling and data security to a mass storage system implemented using flash memory organized into a plurality of blocks wherein each block has a special region for storing its attributes and further in the defect management, defects arising from manufacturing are scanned and defective blocks are marked by altering its attributes (see abstract). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Kikuchi employing a process for marking a defective block in order to identify the defective from the un-defective block as taught by Ma et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to insure the data stored in a memory system be reliable and as a result, the security of the data can be guaranteed (see col. 2, lines 40-44).

5. Claims **2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (U.S. PN: 6,058,047) in view of Ma et al. (U.S. PN: 5,956,473) and further in view of Cooper (U.S. PN; 6,397,357).

As per claims **2 and 3,** Kikuchi in view of Ma et al. teach all the subject matter claimed in claim 1 including Kikuchi teach that each block includes a data region in which data is written and a redundant region in which information indicating the quality of the block, and administrative information such as ECC (error correcting code), used for detecting and

correcting an error occurred in data written and further the ECC used for a purpose that a 1-bit error detected and corrected, and 2-bit error only detected in which designated as a defective block and the re-use thereof is inhibited (disabled) (see col. 1, lines 45-54 and claim 1). Kikuchi in view of Ma et al. **do not teach** a method of suspending an ECC generation. **However,** Copper teach that an ECC generation capabilities of a memory controller are disabled and the ECC check bits will not be generated for data read from and written to system memory (see col. 2, lines 29-32). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Kikuchi in view of Ma et al. including the teachings of Copper to provide a service option in which an ECC suspends or disables generating an ECC codes. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide to facilitate utilization of flexible and efficient memory configurations.

6. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (U.S. PN: 6,058,047).

As per claim **4,** Kikuchi discloses/teaches a semiconductor memory device and a method including a semiconductor memory having a memory region divided into a plurality of blocks including a backup blocks, the number of writes to each block being limited, and a memory controller for reading data from the semiconductor memory so as to check an error in the data read from each block, and correcting the error if it is correctable. Further, the memory controller includes a counter for counting the number of correctable errors detected for each block, transferring the data of the corresponding block to the backup block when the number of errors

detected reaches a preset value (see abstract and col. 1, lines 6-14). Kikuchi teach that each block includes a data region in which data is written and a redundant region in which information indicating the quality of the block, and administrative information such as ECC (error correcting code), used for detecting and correcting an error occurred in data written and further the ECC used for a purpose that a 1-bit error detected and corrected, and 2-bit error only detected designated as a defective block (see col. 1, lines 45-54 and claim 1). Further, Kikuchi discloses/teaches an inhibiting unit which monitors whether or not the count reached a preset value, and if so, transfers the data to the backup block and inhibits the re-use of the block as a defective block (identified as a defective block) (see col. 2, lines 45-52). Kikuchi **do not explicitly** teach a method of searching a defective block. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, the process for searching a defected blocks are required to select the defected block from the un-defected blocks. **Accordingly,** it would have been obvious to one ordinary skill in the art to employ a process for searching defected blocks because such processes would have been required before identifying, marking, and inhibiting the defected blocks.

7. Claims **5-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishino (U.S. PN: 6,526,537) in view of Cooper (U.S. PN; 6,397,357).

As per claim **5,** Kishino a storage capable of generating an ECC for data and adding the ECC to the data to thereby form a read/write unit includes a writing circuit for generating an ECC for N of write data received from a host, adding N equally divided ECC code parts to the N write data, respectively, to thereby form N write units, and writing the N write units to N

continuous addresses of a semiconductor memory device, respectively. A reading circuit gathers the N equally divided ECC code parts contained in read data units read out of the N continuous addresses of the semiconductor memory device to thereby reconstruct the ECC, and corrects errors of the N read data units with the reconstructed ECC (see col. Lines 3-16). Kishino **does not explicitly** teach or disclose an ECC suspension circuit to suspend the ECC generation. **However,** Cooper disclosed a memory controller including a controlling access to a memory device and having error checking and correcting ("ECC") capabilities, an apparatus for verifying the accuracy of said ECC capabilities of the memory controller wherein the apparatus includes means for disabling (suspending) ECC capabilities of the memory controller (see claim 23). Further, Cooper teach an ECC generation capabilities of the memory controller disabled such that ECC check bits will not be generated for data read from and written to system memory (see col. 2, lines 29-32). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to combine (incorporate) the teachings of Kishino with Copper to provide a service option in which an ECC suspends or disables generating an ECC codes. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide to facilitate utilization of flexible and efficient memory configurations.

As per claims **6-9,** Kishino teach all the subject matter claimed in claim 5 including Cooper disclosed a memory controller including a controlling access to a memory device and having error checking and correcting ("ECC") capabilities, an apparatus for verifying the accuracy of said ECC capabilities of the memory controller wherein the apparatus includes means for disabling (suspending) ECC capabilities of the memory controller (see claim 23).

Further, Copper in figure 1 element 13 teaches a bus connected to the ECC memory controller and to other devices (exterior of the memory devices).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,101,614 Gonzales et al.

US PN: 6,412,089 Lenny et al.

US PN: 5,157,670 Kowal

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Gary J. Lamarre
for

Albert DeCady
Primary Examiner